



INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. 050637	Serial No. 10/551,391
	Applicant(s): SASAO, Tsutomu, et al.	
	Filing Date: September 29, 2005	Group Art Unit: Not yet assigned

OTHER DOCUMENTS

_____	BA	Y. Iguchi et al., "Realization of Multiple-Output Functions by Reconfigurable Cascades, " International Conference on Computer Design :VLSI in Computers & Processors (ICCD-2001), Austin, TX, Sept. 23-26, 2001. pp. 388-393 (published page number).				
_____	BB	A. Mishchenko et al., "Encoding of Boolean Functions and Its Application to LUT Cascade Synthesis, " International Workshop on Logic and Synthesis (IWLS2002), New Orleans, Louisiana, June 4-7, 2002, pp.115-120.				
_____	BC	T. Sasao, "Design Methods for Multi-Rail Cascades," International Workshop on Boolean Problems (IWBP2002), Freiberg, Germany, Sept. 19-20, 2002, pp. 123-132.				
_____	BD	T. Sasao et al., "A Design Method for Irredundant Cascades," International Symposium on New Paradigm VLSI Computing, Sendai, Japan, Dec. 12-14, 2002, pp.37-40.				
_____	BE	A. Mishchenko et al., "Logic Synthesis of LUT Cascades with Limited Rails," The Institute of Electronics, Information and Communication Engineers, Lake Biwa, VLD2002-99, November 2002, pp. 1-6.				
_____	BF	H. Gouji et al., "On a Method to Reduce the Number of LUTs in LUT cascades," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLD2001-99, November 2001, 6 sheets, English abstract is included.				
_____	BG	M. Matsuura et al., "Compact Representaions of BDDs for Multiple-Output Functions and Their Optimization," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLS2001-100, November 2001, 6 sheets, English abstract is included.				
<table><tr><td>Examiner</td><td>/Anh Tran/</td><td>Date Considered</td><td>09/08/2008</td></tr></table>			Examiner	/Anh Tran/	Date Considered	09/08/2008
Examiner	/Anh Tran/	Date Considered	09/08/2008			